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APPLICATION

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TITLE: METHOD AND APPARATUS FOR IMPROVING SUPPLY NOISE REJECTION

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PRIORITY: *Under 35 USC 119(e), this application claims priority to U.S. Provisional Patent Application No. 60/470,625, filed on May 15, 2003, which is incorporated herein by reference in its entirety.*

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METHOD AND APPARATUS FOR IMPROVING SUPPLY NOISE REJECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to commonly assigned U.S. Provisional Patent Application No. 60/470,625, filed on May 15, 2003, which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] Electrostatic discharge (ESD) can damage integrated circuits (ICs). ESD is caused when a source of electrostatic potential (e.g., a human body with a static buildup of charge carriers) comes into contact with a circuit input. The electrostatic voltage may damage sensitive ICs if the electrostatic voltage discharges through circuit elements. In order to prevent ESD damage to functional circuits on the IC, ESD protective circuits may be incorporated on the input/output (I/O) pads of the IC. The role of an ESD protection circuit is to ensure, that in case of an ESD event, the electrostatic potential is shunted (or diverted) to ground - i.e., the electrostatic potential can be discharged through the ESD protective circuits, protecting the IC's functional circuits.

[0003] FIG. 1 illustrates a conventional ESD protection scheme for an IC 100 including an I/O pad 102 and an internal circuit 104. The conventional ESD protection scheme includes ESD

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protection circuits 106, 108, and an ESD clamp 110. ESD protection circuits 106, 108 are typically formed by diodes (represented by D1 and D2 in FIG. 1). ESD protection circuit 106 couples I/O pad 102 to a high-side supply VDD 112, and ESD protection circuit 108 couples I/O pad 102 to a low-side supply VSS 114. ESD clamp 110 couples VDD 112 to VSS 114, and provides a discharge path between VDD 112 and VSS 114 during an ESD event.

[0004] There are four types of ESD events that can occur at I/O pad 102 with respect to VDD 112 and VSS 114. The four types of ESD events are:

[0005] (1) I/O pad 102 to VDD 112, positive discharge pulse: An I/O pad 102 to VDD 112 positive discharge pulse occurs when a positive ESD exerts stress on I/O pad 102 with VDD 112 relatively grounded. VSS 114 floats during an I/O pad 102 to VDD 112 positive discharge pulse. As discussed above, the role of an ESD protection circuit is to shunt ESD away from an IC's functional circuits. The I/O pad 102 to VDD 112 positive ESD is shunted away from internal circuit 104 as follows: ESD protection circuit 106 shunts ESD current (associated with the positive discharge pulse) from I/O pad 102 to VDD 112.

[0006] (2) I/O pad 102 to VDD 112, negative discharge pulse: An I/O pad 102 to VDD 112 negative discharge pulse occurs when a negative ESD exerts stress on I/O pad 102 with VDD 112

relatively grounded. VSS 114 floats during an I/O pad 102 to VDD 112 negative discharge pulse. The I/O pad 102 to VDD 112 negative ESD is shunted away from internal circuit 104 as follows: ESD clamp 110 shunts ESD current (associated with the negative discharge pulse) from VDD 112 to VSS 114. ESD protection circuit 108 shunts the ESD current from VSS 114 to I/O pad 102.

[0007] (3) I/O pad 102 to VSS 114, positive discharge pulse: An I/O pad 102 to VSS 114 positive discharge pulse occurs when a positive ESD exerts stress on I/O pad 102 with VSS 114 relatively grounded. VDD 112 floats during an I/O pad 102 to VSS 114 positive discharge pulse. The I/O pad 102 to VSS 114 positive ESD is shunted away from internal circuit 104 as follows: ESD protection circuit 106 shunts ESD current (associated with the positive discharge pulse) from I/O pad 102 to VDD 112. ESD clamp 110 shunts ESD current from VDD 112 to VSS 114.

[0008] (4) I/O pad 102 to VSS 114, negative discharge pulse: An I/O pad 102 to VSS 114 negative pulse occurs when a negative ESD exerts stress on I/O pad 102 with VSS 114 relatively grounded. VDD 112 floats during an I/O pad 102 to VSS 114 negative discharge pulse. The I/O pad 102 to VSS 114 negative ESD is shunted away from internal circuit 104 as follows: ESD

protection circuit 108 shunts ESD current (associated with the negative discharge pulse) from VSS 114 to I/O pad 102.

[0009] The conventional ESD protection scheme described above can generally shunt potentially damaging electrostatic potential away from sensitive circuitry (e.g., internal circuit 104). One limitation of the conventional ESD protection scheme is a large parasitic capacitance that is typically associated with each of ESD protection circuits 106, 108. Such a large parasitic capacitance can couple noise appearing on VDD 112 - i.e., high-side supply noise - through ESD protection circuit 106 to internal circuit 104, and adversely affect the performance and reliability of internal circuit 104.

SUMMARY

[0010] In general, in one aspect, this specification describes an electrostatic discharge (ESD) protection circuit for discharging ESD events. The ESD protection circuit includes an ESD protection circuit having a first and second terminal. The first terminal is coupled to an input/output (I/O) pad, and the second terminal coupled to a low-side supply (VSS). The ESD protection circuit is operable to shunt ESD current during positive and negative ESD events.

[0011] Particular implementations may include one or more of the following features. The ESD protection circuit can include

circuit elements selected from the group consisting of polymer devices, metal oxide silicon (MOS) devices, and diodes. The ESD protection circuit can include two diodes that are in parallel and in opposite directions. The ESD protection circuit can not be directly coupled to a high-side supply (VDD). The ESD protection circuit can further include an ESD clamp to provide a discharge path between the high-side supply (VDD) and the low-side supply (VSS) during an ESD event. The positive and negative ESD events can include an I/O pad to high-side supply (VDD) positive discharge pulse, an I/O pad to high-side supply (VDD) negative discharge pulse, an I/O pad to low-side supply (VSS) positive discharge pulse, and an I/O pad to low-side supply (VSS) negative discharge pulse. The low-side supply (VSS) can float during the I/O pad to high-side supply (VDD) positive discharge pulse and the I/O pad to high-side supply (VDD) negative discharge pulse. The high-side supply (VDD) can float during the I/O pad to low-side supply (VSS) positive discharge pulse and the I/O pad to low-side supply (VSS) negative discharge pulse.

[0012] In general, in another aspect, this specification describes a method for discharging electrostatic discharge (ESD). The method includes receiving a positive or negative discharge pulse on an I/O pad, and shunting ESD current associated with the positive or negative discharge pulse from

the I/O pad to a low-side supply (VSS) prior to shunting the ESD current to a high-side supply (VDD) for all the received positive and negative discharge pulses.

[0013] Particular implementations may include one or more of the following features. The positive discharge pulse can be an ESD event selected from the group consisting of an I/O pad to high-side supply (VDD) positive discharge pulse and an I/O pad to low-side supply (VSS) positive discharge pulse. If the positive discharge pulse is an I/O pad to high-side supply (VDD) positive discharge pulse, shunting ESD current can include shunting ESD current associated with the I/O pad to high-side supply (VDD) positive discharge pulse from the I/O pad to the low-side supply (VSS), then shunting the ESD current from the low-side supply (VSS) to the high-side supply (VDD). If the positive discharge pulse is an I/O pad to low-side supply (VSS) positive discharge pulse, shunting ESD current can include shunting ESD current associated with the I/O pad to low-side supply (VSS) positive discharge pulse from the I/O pad to the low-side supply (VSS).

[0014] The negative discharge pulse can be an ESD event selected from the group consisting of an I/O pad to high-side supply (VDD) negative discharge pulse and an I/O pad to low-side supply (VSS) negative discharge pulse. If the negative discharge pulse is an I/O pad to high-side supply (VDD) negative

discharge pulse, shunting ESD current can include shunting ESD current associated with the I/O pad to high-side supply (VDD) negative discharge pulse from the high-side supply VDD to the low-side supply (VDD), then shunting the ESD current from the low-side supply (VSS) to the I/O pad. If the negative discharge pulse is an I/O pad to low-side supply (VSS) negative discharge pulse, shunting ESD current can include shunting ESD current associated with the I/O pad to low-side supply (VSS) negative discharge pulse from the low-side supply VSS to the I/O pad.

[0015] In general, in another aspect, this specification describes a low noise amplifier (LNA). The LNA includes an RF input and an electrostatic discharge (ESD) protection circuit. The ESD protection circuit includes a first terminal coupled to an input/output (I/O) pad, and a second terminal coupled to a low-side supply(VSS). The ESD protection circuit is operable to shunt ESD current during positive and negative ESD events away from the RF input and through the low-side supply.

[0016] Particular implementations may include one or more of the following features. The low noise amplifier can be compliant with an IEEE standard selected from the group consisting of 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, and 802.11i, and 802.14.

[0017] An ESD protection scheme is provided that protects an internal circuit from high-side supply noise. The ESD

protection scheme does not include an ESD protection circuit that couples the high-side supply to the internal circuit. Thus, there is not a direct path for any high-side supply noise to travel from the high-side supply to the internal circuit. The ESD protection scheme, therefore, provides a better rejection of high-side supply noise.

[0018] The details of one or more implementations are set forth in the accompanying drawings and the description below. Other features and advantages will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0019] FIG. 1 illustrates a conventional ESD protection scheme for an IC.

[0020] FIG. 2 illustrates an ESD protection scheme for an IC.

[0021] FIG. 3 illustrates an ESD protection circuit.

[0022] FIG. 4 is a flowchart of a process for discharging ESD.

[0023] FIG. 5 is schematic diagram of a low noise amplifier (LNA).

[0024] FIG. 6 illustrates an ESD protection circuit for a low noise amplifier.

[0025] FIG. 7 illustrates an ESD protection scheme for an IC.

[0026] FIG. 8 illustrates an ESD protection scheme for ICs within a single supply group.

[0027] FIG. 9 illustrates an ESD protection scheme for ICs within a different supply group.

[0028] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0029] FIG. 2 illustrates an ESD protection scheme for an IC 200 including an I/O pad 202 and an internal circuit 204 that are both immune from high supply noise. The ESD protection scheme includes an ESD protection circuit 206 and an ESD clamp 208, to protect internal circuit 204 from ESD events. ESD clamp 208 couples a high-side supply (VDD 210) to a low-side supply (VSS 212) and provides a discharge path between VDD 210 and VSS 212 during an ESD event. ESD protection circuit 206 couples I/O pad 202 to VSS 212. As shown in FIG. 2, IC 200 does not include an ESD protection circuit to couple I/O pad 202 to VDD 210. Thus, there is not a direct path for any high supply noise (i.e., noise from VDD 210) to travel from VDD 210 to internal circuit 204.

[0030] ESD protection circuit 206 can be formed by polymer devices and/or metal oxide silicon (MOS) devices (e.g., transistors). ESD protection circuit can include diodes (e.g., regular diodes, Zener diodes, TVS (transient voltage suppression) diodes, MOVs (metal oxide varistors), silicon

controlled rectifiers (SCRs), and so on), and be operable to shunt positive and negative ESD current away from internal circuit 204. More specifically, ESD protection circuit 206 provides the following functions upon occurrence of ESD events, as shown in FIG. 2.

[0031] (1) I/O pad 202 to VDD 210, positive discharge pulse: An I/O pad 202 to VDD 210 positive discharge pulse occurs when a positive ESD exerts stress on I/O pad 202 with VDD 210 relatively grounded. VSS 212 floats during an I/O pad 202 to VDD 210 positive discharge pulse. The role of ESD protection circuit 206 is to shunt ESD away from internal circuit 204. The I/O pad 202 to VDD 112 positive discharge pulse is shunted away from internal circuit 204 as follows: ESD protection circuit 206 shunts the ESD current (associated with the positive discharge pulse) from I/O pad 202 to VSS 212. ESD clamp 208 shunts the ESD current from VSS 212 to VDD 210.

[0032] (2) I/O pad 202 to VDD 210, negative discharge pulse: An I/O pad 202 to VDD 210 negative discharge pulse occurs when a negative ESD exerts stress on I/O pad 202 with VDD 210 relatively grounded. VSS 212 floats during an I/O pad 202 to VDD 210 negative discharge pulse. The I/O pad 202 to VDD 112 negative discharge pulse is shunted away from internal circuit 204 as follows: ESD clamp 208 shunts the ESD current (associated with the negative discharge pulse) from VDD 210 to

VSS 212. ESD protection circuit 206 shunts the ESD current from VSS 212 to I/O pad 202.

[0033] (3) I/O pad 202 to VSS 212, positive discharge pulse: An I/O pad 202 to VSS 212 positive discharge pulse occurs when a positive ESD exerts stress on I/O pad 202 with VSS 212 relatively grounded. VDD 210 floats during an I/O pad 202 to VSS 212 positive discharge pulse. The I/O pad 202 to VSS 212 positive discharge pulse is shunted away from internal circuit 204 as follows: ESD protection circuit 206 shunts the ESD current (associated with the positive discharge pulse) from I/O pad 202 to VSS 212.

[0034] (4) I/O pad 202 to VSS 212, negative discharge pulse: An I/O pad 202 to VSS 212 negative discharge pulse occurs when a negative ESD exerts stress on I/O pad 202 with VSS 212 relatively grounded. VDD 210 floats during an I/O pad 202 to VSS 212 negative discharge pulse. The I/O pad 202 to VSS 212 negative discharge pulse is shunted away from internal circuit 204 as follows: ESD protection circuit 206 shunts the ESD current (associated with the negative discharge pulse) from VSS 212 to I/O pad 202.

[0035] FIG. 3 illustrates an implementation of ESD protection circuit 206 formed by a first diode 300 and a second diode 302. As shown in FIG. 3, first diode 300 and second diode 302 are coupled in parallel, and in opposite directions, between I/O pad

202 and VSS 212. That is, first diode 300 has an anode and a cathode coupled to VSS 212 and I/O pad 202, respectively, and second diode 302 has an anode and a cathode coupled to I/O pad 202 and VSS 212, respectively. ESD protection circuit 206, formed by first diode 300 and second diode 302, protects internal circuit 204 from ESD events.

[0036] (1) I/O pad 202 to VDD 210, positive discharge pulse: As discussed above, an I/O pad 202 to VDD 210 positive discharge pulse occurs when a positive ESD exerts stress on I/O pad 202 with VDD 210 relatively grounded. VSS 212 floats during an I/O pad 202 to VDD 210 positive discharge pulse. Second diode 302 shunts the ESD current (associated with the positive discharge pulse) from I/O pad 202 to VSS 212. ESD clamp 208 shunts the ESD current from VSS 212 to VDD 210.

[0037] (2) I/O pad 202 to VDD 210, negative discharge pulse: An I/O pad 202 to VDD 210 negative discharge pulse occurs when a negative ESD exerts stress on I/O pad 202 with VDD 210 relatively grounded. VSS 212 floats during an I/O pad 202 to VDD 210 negative discharge pulse. The I/O pad 202 to VDD 112 negative discharge pulse is shunted away from internal circuit 204 as follows: ESD clamp 208 shunts the ESD current (associated with the negative discharge pulse) from VDD 210 to VSS 212. First diode 300 shunts the ESD current from VSS 212 to I/O pad 202.

[0038] (3) I/O pad 202 to VSS 212, positive discharge pulse: An I/O pad 202 to VSS 212 positive discharge pulse occurs when a positive ESD exerts stress on I/O pad 202 with VSS 212 relatively grounded. (VDD 210 floats during an I/O pad 202 to VSS 212 positive discharge pulse. The I/O pad 202 to VSS 212 positive discharge pulse is shunted away from internal circuit 204 as follows: Second diode 302 shunts the ESD current (associated with the positive discharge pulse) from I/O pad 202 to VSS 212.

[0039] (4) I/O pad 202 to VSS 212, negative discharge pulse: An I/O pad 202 to VSS 212 negative discharge pulse occurs when a negative ESD exerts stress on I/O pad 202 with VSS 212 relatively grounded. VDD 210 floats during an I/O pad 202 to VSS 212 negative discharge pulse. The I/O pad 202 to VSS 212 negative discharge pulse is shunted away from internal circuit 204 as follows: First diode 300 shunts the ESD current (associated with the negative discharge pulse) from VSS 212 to I/O pad 202.

[0040] FIG. 4 shows one implementation of a process 400 for providing an ESD protection scheme for an internal circuit. An ESD event occurs on an I/O pad (step 402). If the ESD event is an I/O pad to VDD, positive discharge pulse, ESD current is first directly shunted from the I/O pad to VSS through an ESD protection circuit (step 404). The ESD current is then directly

shunted from VSS to VDD through an ESD clamp (step 406). If the ESD event is an I/O pad to VDD, negative discharge pulse, ESD current is first directly shunted from VDD to VSS through an ESD clamp (step 408). The ESD current is then directly shunted from VSS to the I/O pad through an ESD protection circuit (step 410). If the ESD event is an I/O pad to VSS, positive discharge pulse, ESD current is directly shunted from the I/O pad to VSS through an ESD protection circuit (step 412). If the ESD event is an I/O pad to VSS, negative discharge pulse, ESD current is directly shunted from VSS to the I/O pad through an ESD protection circuit (step 414).

[0041] The ESD protection scheme illustrated in FIGS. 2 and 3 can be used to protect a wide range of circuits, e.g., a low noise amplifier (LNA). A LNA is a critical building block of an RF transceiver which is sensitive to high-side supply noise. FIG. 5 shows an example of a conventional CMOS LNA 500. CMOS LNA 500 includes an RF input 502. CMOS LNA 500 can be IEEE compliant with the following IEEE standards - 802.11, 802.11a, 802.11b, 802.11e, 802.11g, 802.11h, 802.11i, and 802.14.

[0042] Referring to FIG. 6, ESD protection circuit 206 is particularly suitable to protect LNA circuits due to LNA circuits having relatively low input voltage swings - (e.g., lower than 0.6V - 0.7V). That is, the input voltage swings are

low enough such that neither of diodes 300, 302 are activated by the input voltage swings.

[0043] *Other implementations*

[0044] An internal circuit can have an input that is referenced to a high-side supply VDD instead of a low-side supply VSS - e.g., the internal circuit can have a p-type input device such as a PMOS transistor or a PNP bipolar transistor. In this case, the ESD protection scheme can be modified as shown in FIG. 7, in which case ESD protection circuit 206 couples an internal circuit 700 (having a p-type input device) to high-side supply VDD instead of low-side supply VSS.

[0045] FIG. 8 shows an ESD protection scheme including ESD protection circuits 206A, 206B to protect internal circuits 802, 804 (within a single high-side supply group - i.e., VDD 810) against pin-to-pin zapping between I/O pins 806, 808. For example, an I/O pad 806 to I/O pad 808 positive discharge pulse can occur when a positive ESD exerts stress on I/O pad 806 with I/O pad 808 relatively grounded. In such a case, the role of ESD protection circuits 206A, 206B is to shunt the positive ESD away from internal circuits 802, 804. The positive I/O pad 806 to I/O pad 808 positive discharge pulse is shunted away from internal circuits 802, 804 as follows: ESD protection circuit 206A shunts the ESD current from I/O pad 806 to VSS 812. ESD protection circuit 206B shunts the ESD current from VSS 812 to

I/O pad 808. A positive discharge pulse from I/O pad 808 to I/O pad 806 can similarly be discharged.

[0046] FIG. 9 shows an ESD protection scheme including ESD protection circuits 206A, 206B, and ESD clamps 208A, 208B to protect internal circuits 902, 904 (within different high-side supply groups - i.e., VDD 910, 912) against pin-to-pin zapping between I/O pins 906, 908, and PIN to supply zapping. Pin-to-pin zapping between I/O pins 906, 908 can be discharged as discussed above with respect to the ESD protection scheme of FIG, 8.

[0047] A number of implementations of the invention have been described. Nevertheless, it will be understood that various modifications may be made. For example, the ESD protection scheme can be used to protect circuits having a low input voltage swing (e.g., lower than 0.6V - 0.7V), and a low bias voltage. Also, FIGS. 8 and 9 can have internal circuits that have inputs referenced to a high-side supply VDD instead of a low-side supply VSS. Accordingly, other implementations are within the scope of the following claims.